IN THE CLAIMS

Please amend claim 1 as indicated in the following:

1. (Currently Amended) A method of production testing a video device comprising the steps of:
   mounting a device on a test fixture, wherein the test fixture is coupled to a general-purpose computer;
   testing the device using scan techniques, wherein testing the device includes:
   serially providing a first test vector to the device;
   clocking the device to assert the first test vector within the device;
   serially providing a second test vector to the device;
   receiving results from the first test vector concurrently with ~~the step of~~ providing the second test vector; and
   comparing the results with expected results.
2. (Previously Presented) The method as in Claim 1, wherein the step of testing the device using the scan-test techniques includes the step of determining, after the step of comparing the results, if the device has passed a scan-test, wherein the device has passed the scan-test when the results are equivalent to the expected results and the device has failed the scan-test when the results are different from the expected results.
3. (Previously Presented) The method as in Claim 2, wherein the step of testing the device using the scan-test techniques further includes the step of placing the device in a good bin when the device has passed the scan-test.
4. (Previously Presented) The method as in Claim 3, wherein the device is taken from the good bin for performing the step of testing the device using an at speed test.
5. (Previously Presented) The method as in Claim 2, wherein the step of testing the device using the scan-test techniques further includes the step of placing the device in a bad bin when the device has failed the scan-test.
6. (Original) The method as in Claim 1, wherein the device is a video processing device.

7. (Previously Presented) The method as in Claim 1, wherein the step of serially providing the first test vector to the device includes providing multiple chains of serial test vector values to separate sets of components of the device for concurrently testing the sets of components.

8. (Previously Presented) The method as in Claim 1, further including the steps of:
selecting one of an at speed test mode and a scan-test mode; and
testing the device using an at-speed test when the at speed test mode is selected.

9. (Previously Presented) The method as in Claim 8, wherein the device is tested using the scan techniques before the device is tested using the at speed test.

10. (Original) The method as in Claim 1, wherein the general-purpose computer includes one of a peripheral component interconnect port, an accelerated graphics port, a serial port, a JTAG port, or a parallel port for interfacing with the test fixture.

11. (Previously Presented) A system comprising:

a general purpose computer having:

a data processor having an input/output buffer;

memory having an input/output buffer coupled to the input/output buffer of the data processor, said memory including a set of instructions to provide a scan-test pattern for testing a device;

a communications port having an input/output buffer coupled to the input/output buffer of the data processor;

a test fixture having:

a communications interface coupled to the communications port, the communications port to receive said scan-test pattern;

a scan-chain selector for selecting a particular scan-chain of a plurality of scan chains in said device for testing;

a control module to:

generate signals to set said device in a scan-test mode;

provide said signals to a device socket;

load said scan-test pattern, through said device socket, into said particular scan-chain of said device;

provide a clock signal to said device socket, wherein said clock is to latch output results from said particular scan-chain;

said device socket for interfacing with said device, said device socket to:

provide said signals and scan-test pattern from said control module to said particular scan-chain of said device and;

receive said output results.

12. (Original) The system as in Claim 11, wherein said communications port includes a JTAG port.

13. (Original) The system as in Claim 11, wherein said communications port includes an accelerated graphics port.

14. (Original) The system as in Claim 11, wherein said scan chain selector is configured by a user to select said particular scan chain.

15. (Original) The system as in Claim 11, wherein said scan-chain selector is configured by said set of instructions, through said control module.

16. (Original) The system as in Claim 11, wherein said device includes a graphics processor.

17. (Original) A test fixture comprising:

a bus interface for receiving test signals;

a test mode selector coupled to the bus interface, said test mode selector to route said test signals from said bus interface to one of an at-speed operating path and a scan-test path;

a scan-test control module coupled to said scan-test path of said test mode selector, said scan-test control module to:

engage a scan-test mode in a device;

selecting a particular scan-chain of a plurality of scan-chains associated with said device;

providing a scan pattern to a test socket, wherein said scan pattern is loaded into said scan-chain;

receiving results from said device, wherein results are related to said scan pattern;

a test socket having:

a first input/output buffer coupled to said at-speed operating path of said test mode selector;

a second input/output buffer coupled to said scan-test path of said test mode selector; and

a third input/output buffer coupled buffer coupled to said device.

18. (Original) The test fixture as in Claim 17, wherein said bus interface includes an accelerated graphics port interface.

19. (Original) The test fixture as in Claim 17, wherein said bus interface is coupled to a bus port of an information handling system.

20. (Original) The test fixture as in Claim 17, wherein the test mode selector is configured through said test signals to select from one of the at-speed operating path and the scan-test path.

21. (Original) The test fixture as in Claim 17, wherein the at-speed operating path is used to provide test signals associated with at-speed tests.

22. (Original) The test fixture as in Claim 17, wherein said device includes a graphics processor.